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EXAMINER	
CUTLER, ALBERT H	
ART UNIT	**PAPER NUMBER**
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/811,840	SASAKI, GEN	
	Examiner	Art Unit	
	ALBERT H. CUTLER	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,13-16 and 20-27* is/are pending in the application.

4a) Of the above claim(s) *3-9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,13-16 and 20-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to communication filed on December 15, 2009.

Response to Arguments

2. Applicant's arguments filed December 15, 2009 have been fully considered but they are not persuasive.

3. Applicant argues that there is clearly no disclosure or suggestion of the image processing apparatus of claims 1, 15 and 27 where a compression unit and a storage unit are connected to a bus, and a compression unit outputs compressed image data directly to the storage unit via the bus. The storage unit is external to the image processing part. In contrast, buffer 1140 is part of the architecture/stat structure and is not external. The external memory is described as connected to the line writer 650. Kuo et al. teaches the additional storage steps (into buffers 1140 or 1350) and the use line writer 650, which has additional elements increasing the cost and complexity of the architecture/data structure, increases the processing required and processing time. Moreover, there is no bus described connected to both JPEG hardware 924 and the not shown memory connected to line writer 650. The apparatuses of claims 1, 15 and 27 are neither taught nor suggested by Kuo et al.

4. The Examiner respectfully disagrees. The Examiner interprets the storage unit to be input/output buffer 2 (1140, figure 11), and not any external memory at the output of the line writer (650). Claim 1 recites that the storage unit is outside said image processing part. The Examiner interprets the image processing part to comprise line reader, 620, DSP, 922, ping-pong buffers A and B, 1130, JPEG Hardware, 924, and line

writer, 650 of figure 11. As shown in figure 11, input/output buffer 2 (1140) is clearly outside of the above-defined image processing part. Claim 1 does not require that the storage unit is an external memory connected to the output of line writer (650), but rather simply that it is outside the image processing part. Whether a bus is connected to the not shown memory connected to the line writer (650) is a moot point, as the Examiner has not relied upon any bus connected to a not shown memory connected to the line writer (650). With respect to the bus, amended claim 1 recites "said compression unit is connected to said bus and outputs compressed image data directly to said storage unit via said bus". As shown in figure 11, and detailed in column 11, lines 48-51, the compression unit (JPEG Hardware, 924) outputs compressed image data directly to said storage unit (1140). Kuo et al. teaches that for hardware components "data are transferred across a bus by hardware". JPEG Hardware (924) is a hardware component, as detailed in column 10, lines 53-59. Therefore, the output of compressed image data from the JPEG Hardware (924) to the storage unit (1140) is via a bus.

5. Therefore, the rejection is maintained by the Examiner.

Claim Objections

6. The objections to claims 18 and 19 are hereby removed in view of Applicant's response.

Claim Rejections - 35 USC § 102

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 1, 2, 13-16, 20-25 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuo et al. (US 6,400,471).

9. The Examiner's response to Applicant's arguments, as outlined above, is hereby incorporated into the rejection of claims 1, 2, 13-16, 20-25 and 27 by reference.

Consider claim 1, Kuo et al. teaches:

An image processing apparatus for performing image processing on captured data of an image of a desired subject (see digital camera, 100, figures 1, 2 and 11), comprising:

an image processing part (line reader, 620, DSP, 922, ping-pong buffers A and B, 1130, JPEG Hardware, 924, and line writer, 650, figure 11); and

a storage unit (input/output buffer 2, 1140, figure 11) provided outside said image processing part (see figure 11) and connected to said image processing part by a bus (The compression unit (JPEG hardware, 924) outputs compressed image data directly to the storage unit (1140), figure 11, column 11, lines 48-54. Kuo et al. teaches that the compression unit (JPEG hardware, 924) comprises hardware (column 10, lines 53-62), and that hardware components output data via a bus (column 5, lines 8-10, 116, figure 2). Therefore, Kuo et al. teaches that the compression unit (924) outputs compressed image data directly to a storage unit (1140) via a bus.),

said image processing part (line reader, 620, DSP, 922, ping-pong buffers A and B, 1130, JPEG Hardware, 924, and line writer, 650, figure 11) including:

a buffer memory (ping-pong buffers A and B, 1130, figure 11) for data storage (The buffer memory (1130) stores image data processed by the DSP (922), column 11, lines 34-47.);

an image processing unit (DSP, 922) for performing a predetermined process on said captured data to obtain image data (column 11, lines 34-39), and writing said image data to said buffer memory (The image data is written into the buffer memory (1130) from the DSP (922), column 11, lines 36-38.); and

a compression unit (JPEG hardware, 924) for compressing said image data read from said buffer memory (The image data is compressed using JPEG compression, column 11, lines 34-36, column 7, lines 30-33.) and outputting compressed image data to said storage unit (1140, see figure 11, column 11, lines 48-54), wherein said buffer memory (1130) is connected to receive only said image data from said image processing unit (922) and connected to output said image data only to said compression unit (924, see figure 11, column 11, lines 36-46),

wherein said compression unit is connected to said bus and outputs said compressed data directly to said storage unit via said bus (The compression unit (JPEG hardware, 924) outputs compressed image data directly to the storage unit (1140), figure 11, column 11, lines 48-54. Kuo et al. teaches that the compression unit (JPEG hardware, 924) comprises hardware (column 10, lines 53-62), and that hardware components output data via a bus (column 5, lines 8-10, 116, figure 2). Therefore, Kuo et al. teaches that the compression unit (924) outputs compressed image data directly to a storage unit (1140) via a bus.).

Consider claim 2, and as applied to claim 1 above, Kuo et al. further teaches:

said buffer memory (ping-pong buffers A and B, 1130) includes a first buffer memory (A) and a second buffer memory (B), said image processing apparatus further comprising:

a control unit (CPU, 344, figure 2) being operative (column 5, lines 42-54) in such a manner that while said image processing unit (922) writes said image data either to said first buffer memory (A) or to said second buffer memory (B), said compression unit (924) selectively reads image data previously stored either in said first buffer memory (A) or in said second buffer memory (B) experiencing no writing of said image data by said image processing unit (See column 11, lines 36-46. One buffer is filled with image data from the DSP (922) while the other buffer is output to the JPEG hardware (924).).

Consider claim 13, and as applied to claim 1 above, Kuo et al. further teaches:

a first switching unit connected between said image processing unit and said buffer memory; and a second switching unit connected between said compression unit and said buffer memory (As the image data is alternately read into and out of the ping-pong buffers (1130), there must be a first switching unit connected between said image processing unit (922) and said buffer memory (1130), and a second switching unit connected between said compression unit (924) and said buffer memory (1130), column 11, lines 36-46.).

Consider claim 14, and as applied to claim 13 above, Kuo et al. further teaches:

said buffer memory (1130) comprises first and second buffer memories (A and B) connected in parallel (As parallel operations are performed involving buffer memories A and B, they are connected in parallel, column 11, lines 38-46.).

Consider claim 22, and as applied to claim 1 above, Kuo et al. further teaches:

said image processing part comprises:

a first processing unit (line reader, 620) for performing a first processing on said captured data and for storing first processed data in said storage unit (The line reader (620) reads said captured data and stores first processed data in the input/output buffer 1 (1120) of said storage unit, column 11, lines 31-36.); and

a second processing unit (DSP, 922) for performing a second processing on said first processed data obtained from said storage unit (1120) and outputting said image data to said buffer memory (The DSP (922) processes data obtained from the input/output buffer 1 (1120), and outputs the processed data to said buffer memory (1130), column 11, lines 34-46.).

Consider claim 23, and as applied to claim 1 above, Kuo et al. further teaches:

said image processing part (see 924 and 650, figure 11) is connected to store data in and retrieve data from said storage unit (Image data is stored in and retrieved from input/output buffer 2 (1140, figure 11), column 11, lines 48-51.).

Consider claim 24, and as applied to claim 1 above, Kuo et al. further teaches:

said compression unit (924) compressing said image data read from said buffer memory (1130) and storing said image data in said storage unit (The compression unit (924) reads data from the buffer memory (1130) and stores the data in the input/output buffer 2 (1140), figure 11, column 11, lines 36-51.).

Consider claim 25, and as applied to claim 1 above, Kuo et al. further teaches that said buffer memory comprises two line buffers each having a length not less than a length of image data processed by said image processing unit a single time (The image processing unit processes lines of image data, column 11, lines 7-54. Column 10, lines 36-40 detail that that the JPEG processing accepts lines of data as its input. Column 11, lines 36-39 detail that the ping–pong buffers are used such that the DSP (922) and JPEG hardware (924) can be run in parallel. Thus each ping-pong buffer (A and B) must have a length not less than a line of image data.).

Consider claim 15, Kuo et al. teaches:

An image processing apparatus for performing image processing on captured data of an image of a desired subject (see digital camera, 100, figures 1, 2 and 11), comprising:

an image processing part (line reader, 620, DSP, 922, ping-pong buffers A and B, 1130, JPEG Hardware, 924, and line writer, 650, figure 11); and

a storage unit (input/output buffer 1, 1120, and input/output buffer 2, 1140, figure 11) provided outside said image processing part (see figure 11) and connected to said image processing part by a bus (The compression unit (JPEG hardware, 924) outputs compressed image data directly to the storage unit (1140), figure 11, column 11, lines 48-54. Kuo et al. teaches that the compression unit (JPEG hardware, 924) comprises hardware (column 10, lines 53-62), and that hardware components output data via a bus (column 5, lines 8-10, 116, figure 2). Therefore, Kuo et al. teaches that the compression unit (924) outputs compressed image data directly to a storage unit (1140) via a bus.),

said image processing part (line reader, 620, DSP, 922, ping-pong buffers A and B, 1130, JPEG Hardware, 924, and line writer, 650, figure 11), including:

first and second buffer memories (ping-pong buffers A and B, 1130) connected in parallel for data storage (The buffer memory (1130) stores image data processed by the DSP (922), column 11, lines 34-47. As parallel operations are performed involving buffer memories A and B, they are connected in parallel, column 11, lines 38-46.);

an image processing unit (DSP, 922) for performing a predetermined process on said captured data to obtain image data (column 11, lines 34-39), and alternatingly writing said image data to said first and second buffer memories (Image data is alternately written into ping-pong buffers A and B from the DSP (922), column 11, lines 36-46.); and

a compression unit (JPEG hardware, 924) for compressing said image data alternatingly read from said first and second buffer memories (The image data is

alternately read from ping-pong buffers A and B (column 11, lines 36-46), and compressed using JPEG compression, column 11, lines 34-36, column 7, lines 30-33.),

wherein said first and second buffer memories (A and B, 1130) are connected to receive only said image data from said image processing unit (922) and connected to output said image data only to said compression unit (924, see figure 11, column 11, lines 36-46), and said compression unit (924) is connected to said bus and outputs compressed image data directly to said storage unit via said bus (The compression unit (JPEG hardware, 924) outputs compressed image data directly to the storage unit (1140), figure 11, column 11, lines 48-54. Kuo et al. teaches that the compression unit (JPEG hardware, 924) comprises hardware (column 10, lines 53-62), and that hardware components output data via a bus (column 5, lines 8-10, 116, figure 2). Therefore, Kuo et al. teaches that the compression unit (924) outputs compressed image data directly to a storage unit (1140) via a bus.).

Consider claim 16, and as applied to claim 15 above, Kuo et al. further teaches:

a first switching unit connected between said image processing unit and said first and second buffer memories; and a second switching unit connected between said compression unit and said first and second buffer memories (As the image data is alternately read into and out of the ping-pong buffers (1130), there must be a first switching unit connected between said image processing unit (922) and said first and second buffer memories (1130), and a second switching unit connected between said

compression unit (924) and said first and second buffer memories (1130), column 11, lines 36-46.).

Consider claim 20, and as applied to claim 15 above, Kuo et al. further teaches:

said image processing part (see 924 and 650, figure 11) being connected to store data in and retrieve data from said storage unit (Image data is stored in and retrieved from input/output buffer 2 (1140, figure 11), column 11, lines 48-51.).

Consider claim 21, and as applied to claim 15 above, Kuo et al. further teaches:

said image processing part comprises:

a first processing unit (line reader, 620) for performing a first processing on said captured data and for storing first processed data in said storage unit (The line reader (620) reads said captured data and stores first processed data in the input/output buffer 1 (1120) of said storage unit, column 11, lines 31-36.); and

a second processing unit (DSP, 922) for performing a second processing on said first processed data obtained from said storage unit (1120) and outputting said image data to said buffer memory (The DSP (922) processes data obtained from the input/output buffer 1 (1120), and outputs the processed data to said buffer memory (1130), column 11, lines 34-46.).

Consider claim 27, Kuo et al. teaches:

An image processing apparatus for performing image processing on captured data of an image of a desired subject (see digital camera, 100, figures 1, 2 and 11), comprising:

an image processing part (line reader, 620, DSP, 922, ping-pong buffers A and B, 1130, JPEG Hardware, 924, and line writer, 650, figure 11); and

a storage unit (input/output buffer 2, 1140, figure 11) provided outside said image processing part (see figure 11) and connected to said image processing part by a bus (The compression unit (JPEG hardware, 924) outputs compressed image data directly to the storage unit (1140), figure 11, column 11, lines 48-54. Kuo et al. teaches that the compression unit (JPEG hardware, 924) comprises hardware (column 10, lines 53-62), and that hardware components output data via a bus (column 5, lines 8-10, 116, figure 2). Therefore, Kuo et al. teaches that the compression unit (924) outputs compressed image data directly to a storage unit (1140) via a bus.),

said image processing part (line reader, 620, DSP, 922, ping-pong buffers A and B, 1130, JPEG Hardware, 924, and line writer, 650, figure 11), including:

an image processing unit (line reader, 620 and DSP, 922, figure 11) for performing a predetermined process on said captured data to obtain image data (Predetermined processes performed on the captured data are detailed in column 11, lines 29-38.);

a line memory (620) integrated into said image processing unit (See figure 11, column 11, lines 29-36.);

a compression unit (JPEG hardware, 924) for compressing said image data (The image data is compressed using JPEG compression, column 11, lines 34-36, column 7, lines 30-33.); and

a buffer memory (ping-pong buffers A and B, 1130, figure 11) connected between said image processing unit (620, 922) and said compression unit (924, see figure 11);

a DMA controller controlling transfer of compressed image data between the compression unit and the storage unit (Kuo et al. teaches that the JPEG hardware (i.e. the compression unit) can be replaced with an image processing hardware system (1230, figure 13) with extended functionality, column 11, line 63 through column 12, line 9. The hardware architecture is DMA based, column 12, lines 10-24. A DMA engine (1430, i.e. DMA controller) is set up for executing the image processing and output to the line writer (650) and the storage unit, column 12, lines 59-67. Figure 14 shows that the DMA controller (1430) outputs data to the line writer (650) and thus the storage unit.),

wherein said buffer memory (1130) is connected to receive only said image data from said image processing unit (620, 922) and connected to output said image data only to said compression unit (924, see figure 11, column 11, lines 36-46), and compressed image data is output directly from said compressing unit via said bus to said storage unit, and said compression unit is connected to said bus (The compression unit (JPEG hardware, 924) outputs compressed image data directly to the storage unit (1140), figure 11, column 11, lines 48-54. Kuo et al. teaches that the compression unit

(JPEG hardware, 924) comprises hardware (column 10, lines 53-62), and that hardware components output data via a bus (column 5, lines 8-10, 116, figure 2). Therefore, Kuo et al. teaches that the compression unit (924) outputs compressed image data directly to a storage unit (1140) via a bus.).

Claim Rejections - 35 USC § 103

10. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

11. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuo et al. (US 6,400,471) in view of Eglit (US 6,002,446).

Consider claim 26, and as applied 1 above, Kuo et al. further teaches that said image processing unit comprises a line memory (input/output buffer, 1120) for storing said captured data (The line memory (1120) stores data output from the line reader (620), column 11, lines 34-36.), and that said buffer memory comprises two line buffers each having a length not less than a length of image data processed by said image processing unit a single time (The image processing unit processes lines of image data, column 11, lines 7-54. Column 10, lines 36-40 detail that that the JPEG processing accepts lines of data as its input. Column 11, lines 36-39 detail that the ping–pong buffers are used such that the DSP (922) and JPEG hardware (924) can be run in parallel. Thus each ping-pong buffer (A and B) must have a length not less than a line of image data.).

However, Kuo et al. does not explicitly teach that each line buffer has a length not more than a length of said line memory.

Eglit similarly teaches an image processing apparatus (figure 4, column 11, lines 27-42) with ping pong buffers (420, column 12, lines 14-18).

However, in addition to the teachings of Kuo et al., Eglit teaches that each line buffer has a length not more than a length of said line memory (Eglit teaches that the line buffer (420) comprises "two lines" arranged and viewed as two banks. Thus each buffer has a length of one line.).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to have each line buffer taught by Kuo et al. have a length not more than a length of said line memory as taught by Eglit for the benefit of saving on memory requirements.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALBERT H. CUTLER whose telephone number is (571)270-1460. The examiner can normally be reached on Mon-Thu (9:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sinh Tran/
Supervisory Patent Examiner, Art Unit 2622

AC